IN THE CLAIMS

1-27. (Cancelled)

28. (Currently amended) A semiconductor package comprising:

a substrate having a plurality of first printed circuit bond fingers formed on the surface of the substrate ~~mounted thereon~~;

a semiconductor chip having a plurality of bond pads formed thereon;

a plurality of first printed circuit solder ball pads ~~mounted~~ formed on the surface of the substrate;

a printed circuit pattern formed on the surface of the substrate between each of a group of first printed circuit bond fingers and a corresponding first solder ball pad;

a wire bond formed between each of the group of first printed circuit bond fingers and a corresponding bond pad thereby electrically connecting each of the corresponding bond pads to a first solder ball pad;

a second printed circuit bond finger formed on the surface of the substrate;

a second printed circuit solder ball pad formed on the surface of the substrate;

a ~~first bond finger having a conductive~~ printed circuit pattern formed on the surface of the substrate between the second printed circuit bond finger and ~~connecting it to one of~~ the second printed circuit solder ball pads~~.~~;

a third printed circuit bond finger formed on the surface of the substrate;

~~a second bond finger having~~ a ~~first~~ wire bond~~ing unit connecting it~~ having one end affixed to the third bond finger and the other end affixed to one of the bond pads; and

a ~~second~~ wire bond~~ing unit connecting~~ having one end affixed to the ~~first~~ second bond finger and the other end affixed to the ~~second~~ third bond fingers thereby electrically connecting said one bond pad to said ~~one~~ second printed circuit solder ball pad.

29. (Currently amended) The semiconductor package of claim 28 wherein there is no ~~conductive~~ printed circuit pattern between the ~~second~~ third bond finger and any of the solder ball pads.

30. (Currently amended) The semiconductor package of claim 29 where there is no wire bond~~ing unit~~ between the ~~first~~ seeond bond finger and any of the bond pads.

31. (Currently amended) The semiconductor package of claim 28 where there is no wire bond~~ing unit~~ between the ~~first~~ second bond finger and any of the bond pads.

32. (Currently amended) The semiconductor package of claim 28, further comprising:

an encapsulant for encapsulating the semiconductor chip and wire bond~~sing units~~.

33. (Currently amended) The semiconductor package of claim 32, further comprising:

a solder ball connected to said ~~one~~ second printed circuit solder ball pad.

34. (Currently amended) The semiconductor package of claim 28, wherein the substrate is a single-layer substrate on which the printed circuit pattern is formed.

35. (Previously presented) The semiconductor package of claim 28, wherein the substrate is a double-layer substrate or a multi-layer substrate.

36. (Currently amended) The semiconductor package of claim 28, wherein a solder mask is not formed on the ~~first~~ second bond finger.

37. (Currently amended) The semiconductor package of claim 28, wherein the ~~second~~ wire bond~~sing unit is~~ are formed over the substrate.

38. (Currently amended) The semiconductor package of claim 28, wherein the second wire bond~~ing unit~~ between the second bond finger and the third bond finger is formed on an outer region of the substrate on which the semiconductor chip is mounted.

39. Canceled.

40. (Previously presented) The semiconductor package of claim 28, wherein the semiconductor chip is attached to the substrate using an adhesive.

41. Canceled.

42. (Currently amended) The semiconductor package of claim 28, wherein the first bond fingers ~~has~~ have the same pad shape as that of the second bond finger.

43. (Currently amended) A semiconductor package comprising:

a substrate having a plurality of printed circuit bond fingers formed on the surface of the substrate ~~mounted thereon~~;

a plurality of printed circuit solder ball pads ~~mounted~~ formed on the surface of the substrate;

a first ~~conductive~~ printed circuit pattern connected to one of the solder ball pads;

a second ~~conductive~~ printed circuit pattern connected to one of the bond fingers; and

a wire bond~~ing unit connecting~~ having one end affixed to the first printed circuit pattern and the other end affixed to the second ~~conductive~~ printed circuit patterns thereby connecting said one bond pad to said one solder ball pad.

44. (Currently amended) The semiconductor package of claim 43, further comprising:

an encapsulant for encapsulating the semiconductor chip and the wire bond~~ing unit~~.

45. (Previously presented) The semiconductor package of claim 44, further comprising:

a solder ball connected to the said one solder ball pad.

46. (Currently amended) The semiconductor package of claim 43, wherein the first and second printed circuit patterns each have a width that enables wire bonding to be performed thereon.